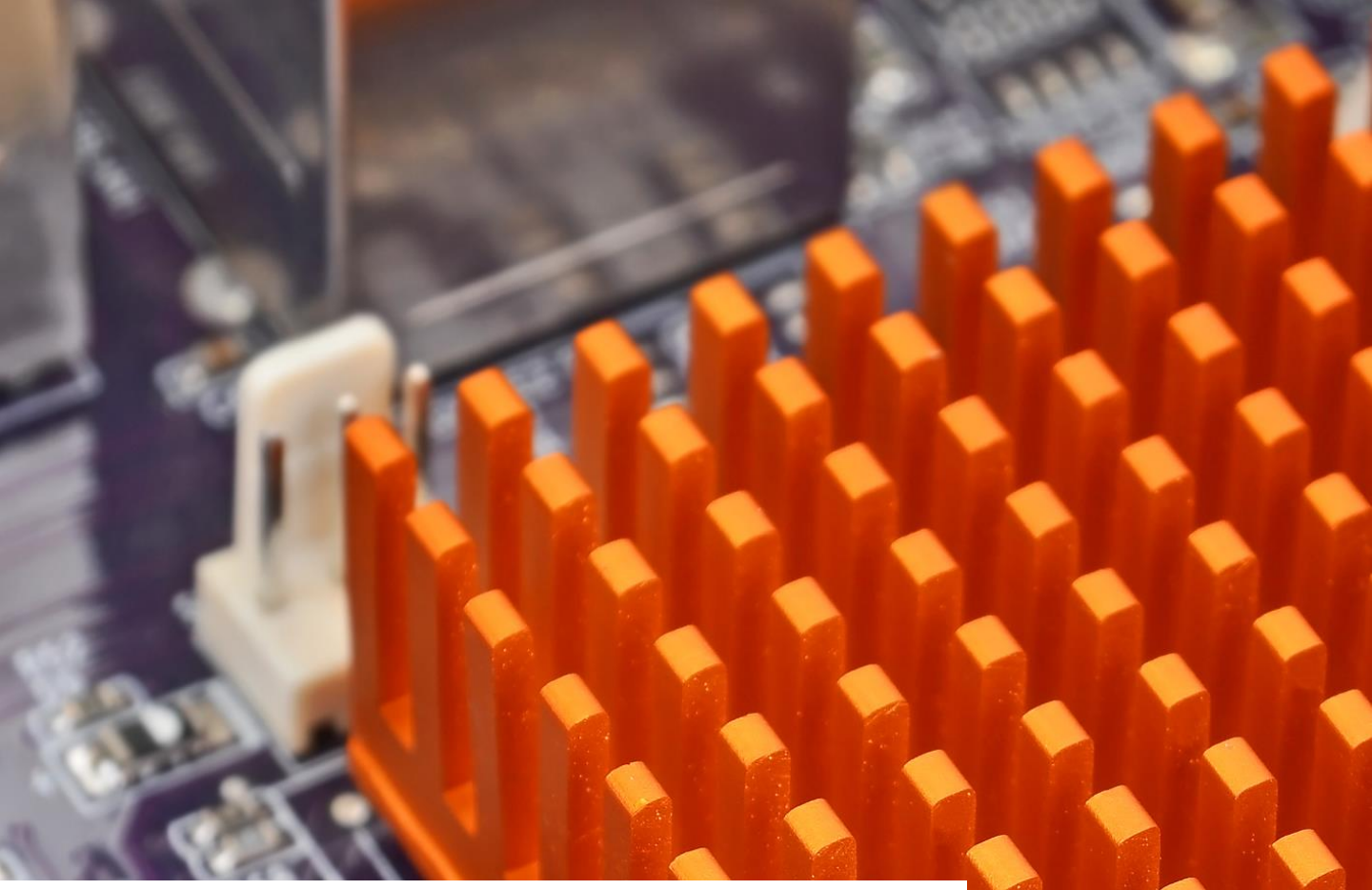


FPGA WEEK 2024

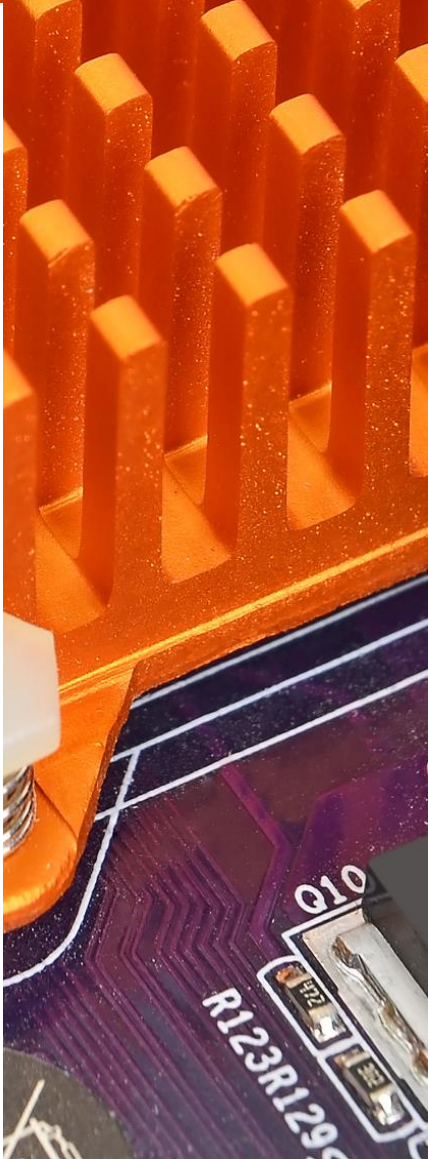
October 22-25

altera
An Intel Company

LATTICE SEMICONDUCTOR

MICROCHIP

ARROW



FPGA WEEK 2024

Arrow is pleased to invite you to the second edition of **ARROW FPGA WEEK** in Parma (once your registration will be confirmed you will receive all the information needed to participate to the event).

The event will give you the opportunity to learn all news and updates from **Arrow FPGA suppliers: Altera, Lattice and Microchip**.
The event is dedicated to senior and beginner FPGA designers. During the workshop, participants will get an overview and perform exercises on FPGA evaluation boards provided by Arrow.

During the first 3 days the sessions will be depth technical with presentation and more practical parts (hands-on) where participants will have the opportunity to perform the exercises on their own PCs.
The last morning will be more theoretical with a basis Verilog/system Verilog training.

Sessions are repeated to allow everyone to participate avoiding having many people during hands-on. Anyone will have the opportunity to perform all sessions. **The event is limited in number.**

During the event, the showcase will host:
Altera, AEI, Diodes, DVS, Engicam, EVERSPIN, GEB, Lattice, Lauterbach, Mas Elettronica, Microchip, Micron, Molex, SCAI CONNECT, Sanitas EG, Skyworks, TDK, Var Industries and XJTAG.

The event is limited in number, after completing your registration your participation will be confirmed via email before October 2nd, 2024.

Contact Reference:
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October 22, 2024

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<tr><td>12:30 – 13:30</td><td colspan="2">Lunch</td><td rowspan="8">Showcase</td></tr>
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Altera – Quartus Prime tutorial (1)
During this session customers can see an overview about Altera Quartus Prime Lite FPGA development tool. The purpose of the training is to take confidence about FPGA development methods (Source Code, Synthesys, Timing Analysis, Fitting and Assembler) and Verification tools available (Simulation and Debug).
The exercise will involve users creating a project from scratch following a consolidated tutorial named “My First FPGA”. Users will learn how to navigate through Quartus Prime GUI and tools to create and build a simple FPGA project.

Lattice - Radiant Basic tutorial (1)
Corporate Overview - product positioning - supply resiliency - products lifetime.
Basic use exercise of Radiant. During the exercise the following steps will be carried out:Create a new Radiant software project:

- Customize IP using IP Catalog.
- Verify functionality with simulation.
- Set timing and location constraints.
- Process the design.
- Analyze power consumption.
- Analyze static timing.
- Create on-chip debug logic.
- Download a bitstream to an FPGA.
- Perform logic analysis.

Microchip - Libero® SoC training (1)
This session presents an overview of the Microchip PolarFire® FPGA and Libero® SoC tool, emphasizing its advanced debugging capabilities, which are critical for developing high-performance applications in communications, defense, and industrial automation.
Participants will dive into a comprehensive hands-on experience, learning how to navigate and leverage Libero® SoC for efficient project development, integrating various peripherals within the FPGA fabric. The session will showcase the advanced capabilities of SmartDebug, a tool for debugging fabric, transceivers and memory content, available in the Libero® SoC design suite. SmartDebug simplifies real-time functional verification with features such as live probing and usage of hardware breakpoints that are crucial for an efficient debugging process.

October 23, 2024

	AMELIA	AUDITORIUM	GILDA A/B
08:45 – 09:00	**Welcome Coffee Registration**		**Showcase**
09:00 – 10:45	**Altera –** Nios V implementation (2)	**Microchip -** Polarfire® SoC multicore RiscV hands-on (2)	
10:45 – 11:15	**Break**		
11:15 – 13:00	**Lattice -** La piattaforma NEXUS 28 nm FDSOI + Esercitazione Lattice RiscV MC (2)	**Altera –** Nios V implementation (2)	
13:00 – 14:00	**Lunch**		
14:00 – 14:30		**Speech - XJTAG -** What is JTAG and how can JTAG help me?	
14:30 – 15:00		**Speech - G.E.B. Enterprise -** State of the art design and manufacturing verification methods	
15:00 – 15:15	**Break**		
15:15 – 17:00	**Microchip -** Polarfire® SoC multicore RiscV hands-on (2)	**Lattice -** La piattaforma NEXUS 28 nm FDSOI + Esercitazione Lattice RiscV MC (2)	
17:00 – 17:30		**Speech - Advanced Energy** Power Conversion Architectures and modules for generating low voltage, high current power supply rails for Target Devices	
17:30 – 18:00		**Speech TDK** - µPOL™ Chip-Embedded DC-DC Power Modules	
From 19:00	**Microchip Dinner - Parmigiano Reggiano Experience Dinner Event**		

Altera – Nios V implementation (2)
This session will offer an overview about new NiosV SoftCore (plus Peripherals). The NiosV is is based on RiscV architecture: Nios V/g: General Purpose Processor is based on RV32IM(F)Zicsr_Zicbom instruction set. It's the highest performance softcore and support RTOS embedded system.
Nios V/m: Microcontroller is based on RV32IZcsr (Pipelined or Non-Pipelined) instruction sets. It's balanced solution for performance/size, it supports RTOS embedded system Nios V/c: Compact Microcontroller it's based on RV32I instruction set. Use it for non-interrupt driven control applications.

Lattice – Platform NEXUS 28 nm FDSOI. Exercise hands-on Lattice RiscV MC (2)
The 28 nm Lattice Nexus technology FPGAs combine characteristics of high reliability, very low power consumption and small package dimensions. The NEXUS FPGA offering ranges from 9K to 100K LUTs, integrated HW peripherals such as PCI express gen3, MIPI up to 2.5Gbps, ADC converters in packages up to 4x4mm.
A RiscV MC Lattice Processor-based system will be created using the Lattice Propel development system. During the exercise, the integration of a custom peripheral will be performed step-by-step starting from the source code, simulation and on-board HW debugging.

Microchip - Polarfire® SoC multicore RiscV hands-on (2)
This session offers an overview of the PolarFire® SoC, featuring a multi-core 64-bit RISC-V processor that supports rich operating systems like Linux® and Asymmetric Multiprocessing (AMP), blending FPGA flexibility with the efficiency of a hardened processor.
In the practical segment, participants will use the processor in bare-metal mode for custom peripheral access within the fabric. The exercise will provide insights into hardware resource control and management, including unauthorized access protection through Physical Memory Protection. The session will also illustrate the process of porting the same application to a Linux environment. The tutorial emphasizes the versatility of the device, showing how applications can evolve from a simple bare-metal framework to a sophisticated Linux system, providing a comprehensive view of system development on PolarFire® SoC.

October 24, 2024

	AMELIA	AUDITORIUM	GILDA A/B
08:45 – 09:00	**Welcome Coffee Registration**		**Showcase**
09:00 – 10:45	**Microchip -** Polarfire® serdes hands-on (3)	**Altera –** Agilex5 GHRD Hands-On (3)	
10:45 – 11:15	**Break**		
11:15 – 13:00	**Lattice -** La piattaforma AVANT 16 nm + Esercitazione Lattice RiscV RX + LPDDR4 (3)	**Microchip -** Polarfire® serdes hands-on (3)	
13:00 – 14:00	**Lunch**		
14:00 – 14:30		**Speech Skyworks -** Clock Management in the latest generation FPGAs	
14:30 – 15:00		**Speech Lauterbach** - One System to rule them all: Lauterbach TRACE32 for Lattice, Microchip and Intel FPGA SoCs	
15:00 – 15:15	**Break**		
15:15 – 17:00	**Altera –** Agilex5 GHRD Hands-On (3)	**Lattice -** La piattaforma AVANT 16 nm + Esercitazione Lattice RiscV RX + LPDDR4 (3)	
17:00 – 17:30		**Open Speech**	
17:30 – 18:00		**Open Speech**	
From 20:30	**Altera Dinner - Street Food Dinner Event**		

Altera – Agilex5 GHRD Hands-On (3)
The section is designed to explore Agilex5E FPGA features in terms of high-speed system clock Fabric and Multicore Cortex A56 and A72 CPUs (HPS – Hard Processor System).

During the session several Agilex5E – Eagle devkits will be available to physically implement the GHRD project ont the board and looking for the results

Lattice - Platform AVANT 16 nm + Esercitazione Lattice RiscV RX + LPDDR4 (3)
Lattice proposes mid-range FPGAs in AVANT 16 nm technology. The AVANT platform offers "best in class" reliability, safety and consumption. It integrates features such as 25 GBps SERDES, PCI express gen4 HW, memory interfaces up to DDR5 and a high number of DSPs.
A system based on RiscV RX Lattice Processor with LPDDR4 external memory will be created. System based on the GHRD/GSRD lattice reference design:

- RISC-V RX Soft CPU
- QSPI Flash Controller and on Chip Memory
- ABP connected UART, GPIO and LED output
- Multi Port Memory LPDDR4 Controller support
- Gigabit Ethernet interface and SGDMA data transfer IP "

Microchip - Polarfire® serdes hands-on (3)
This session is designed to provide an in-depth understanding of the embedded high-speed transceiver blocks within the PolarFire® FPGA, capable of data rates ranging from 250 Mbps to 12.7 Gbps with industry-leading power consumption performance.
The hands-on portion of the session will guide participants through the implementation of a design using the PolarFire® high-speed transceivers. Attendees will gain practical experience in configuring and deploying these transceivers, including simulating the entire project. Participants will employ SmartDebug to generate the eye diagram, an essential tool for analyzing signal integrity and ensuring the optimal performance of the transceivers. To conclude, attendees will learn how to verify power consumption using a Power Monitor tool, highlighting the power efficiency of the PolarFire® FPGA family.

October 25, 2024

	AUDITORIUM
08:45 – 09:00	**Welcome Coffee Registration**
09:00 – 11:00	Verilog / SysVerilog
11:00 – 11:15	**Break**
11:15 – 12:45	Verilog / SysVerilog or Simulation tools
13:30 – 14:30	**Lunch**
14:30	**Wrap up and Closure**

Pre- register Now

This is a pre-registration, your participation
will be confirmed by email before October 2, 2024.

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Speech - October 22, 2024

- **Molex - BittWare Hardware and Partners Help De-risk Your FPGA Project**

We know FPGAs bring high performance but there's risk there too—design for these devices is notoriously complex. Although some progress has been made with higher-level tools, BittWare still sees many of our customers using native FPGA tools and approaches.
That's why we launched a Partner program to help customers choose best-in-class partners and collaborate to build specific solutions. Customers reduce risk by choosing a COTS option and save development by using partner IP/frameworks. We'll talk through our portfolio of hardware and partners, and the benefits of each.

- **VAR Industries - Questa-Driven Verification Flows for High-Quality FPGA Design**

This presentation addresses the challenges of verifying complex FPGA designs in the era of high-speed protocols and intricate system-on-chip architectures. It provides an overview of the Siemens Questa Design Solutions covering both simulation and formal methods to ensure high-quality, reliable FPGA design.

Speech - October 23, 2024

- **XJTAG - What is JTAG and how can JTAG help me?**

JTAG is typically used for 3 things: CPU debug, in-circuit programming and test.
About test, JTAG effectively turns the pins on enabled devices (i.e. FPGAs, processors and CPLDs) into virtual test probes that can all be electronically accessed through a single JTAG connection. These virtual probes give you direct control of the pins, so you do not need to understand the device's internal functionality.
Therefore, JTAG can be used from prototype to manufacture and even across projects.
This talk will introduce the technology and gives examples of how a dedicated boundary scan test software can unlock the full capability of JTAG, providing you with an easy-to-use method to test and program boards.

- **Advanced Energy - Power Conversion Architectures and modules for generating low voltage, high current power supply rails for Target Devices**

Content will cover the following;

- Challenges of power delivery at low-voltage, high current
- Power-Architectures from different common voltages to the low-voltage, high current rails required.
- Transient load requirements.
- Realization of solutions to achieve the objectives.

- **G.E.B. Enterprise - State of the art design and manufacturing verification methods**

With a 65 years history on PLD/FPGA design and JTAG testing, we offer state of the art design and manufacturing verification methods. These methods are also applicable to Gigabit interfaces, such as PCIe.
Methods of integration is the solution!

- **TDK - µPOL™ Chip-Embedded DC-DC Power Modules**

Abstract: µPOL™ product family are chip embedded power modules for compact DC-DC power solutions from 1A to 200A. This is designed to power modern microprocessors, microcontroller, ASIC, FPGA, DSP and advanced digital logic devices. Intro to Qspice and Simplis design tool library for FPGA power.

Speech - October 24, 2024

- **One System to rule them all: Lauterbach TRACE32 for Lattice, Microchip and Intel FPGA SoCs**

Abstract: Lattice, Microchip and Intel FPGA SoCs offer extraordinary power and flexibility, but utilizing them without advanced debug and trace tools can be challenging. Lauterbach TRACE32 is the ideal solution to unlock the full potential of these SoCs. Our systems provide comprehensive support for program tracing, digital and analog signal tracking, FPGA programming, and extensive support for operating systems and hypervisors, ensuring effective management of multicore environments for Arm Cortex, RISC-V, NIOS-II, and Mico32 architectures. TRACE32 enables precise timing analysis and requirement verification, ensuring your system meets all necessary specifications. Trace-based code coverage is a key tool for safety-critical certifications. Optimize your FPGA SoC development workflow with TRACE32 and discover how to accelerate software development.

- **Skyworks - Clock Management in the latest generation FPGAs**

The precision requirements of various peripherals and how to generate all references with a single device.